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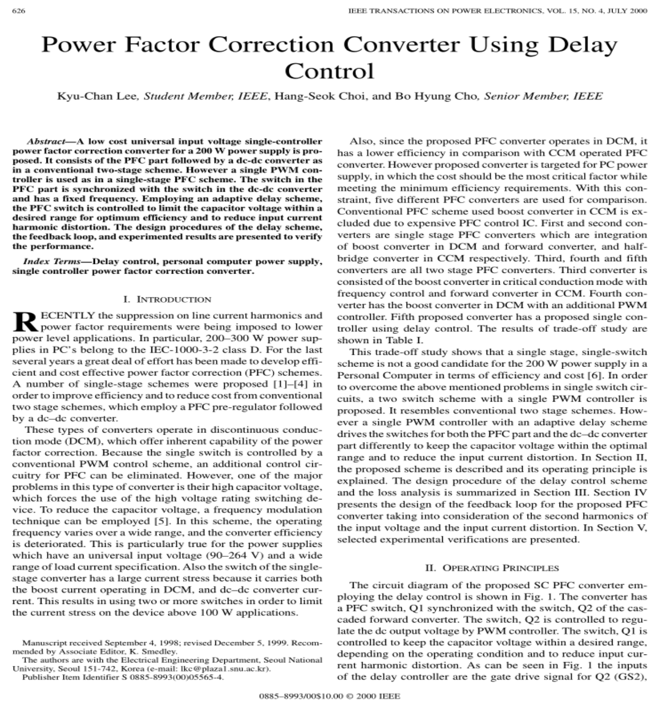

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Power Factor Correction Converter Using Delay Control

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***Abstract*—A low cost universal input voltage single-controller power factor correction converter for a 200 W power supply is proposed. It consists of the PFC part followed by a dc-dc converter as in a conventional two-stage scheme. However a single PWM controller is used as in a single-stage PFC scheme. The switch in the PFC part is synchronized with the switch in the dc-dc converter and has a fixed frequency. Employing an adaptive delay scheme, the PFC switch is controlled to limit the capacitor voltage within a desired range for optimum efficiency and to reduce input current harmonic distortion. The design procedures of the delay scheme, the feedback loop, and experimented results are presented to verify the performance.**

***Index Terms*—Delay control, personal computer power supply, single controller power factor correction converter.**

I. INTRODUCTION

RECENTLY the suppression on line current harmonics and power factor requirements were being imposed to lower power level applications. In particular, 200–300 W power supplies in PC's belong to the IEC-1000-3-2 class D. For the last several years a great deal of effort has been made to develop efficient and cost effective power factor correction (PFC) schemes. A number of single-stage schemes were proposed [1]–[4] in order to improve efficiency and to reduce cost from conventional two stage schemes, which employ a PFC pre-regulator followed by a dc–dc converter.

These types of converters operate in discontinuous conduction mode (DCM), which offer inherent capability of the power factor correction. Because the single switch is controlled by a conventional PWM control scheme, an additional control circuitry for PFC can be eliminated. However, one of the major problems in this type of converter is their high capacitor voltage, which forces the use of the high voltage rating switching device. To reduce the capacitor voltage, a frequency modulation technique can be employed [5]. In this scheme, the operating frequency varies over a wide range, and the converter efficiency is deteriorated. This is particularly true for the power supplies which have an universal input voltage (90–264 V) and a wide range of load current specification. Also the switch of the single-stage converter has a large current stress because it carries both the boost current operating in DCM, and dc–dc converter current. This results in using two or more switches in order to limit the current stress on the device above 100 W applications.

Also, since the proposed PFC converter operates in DCM, it has a lower efficiency in comparison with CCM operated PFC converter. However proposed converter is targeted for PC power supply, in which the cost should be the most critical factor while meeting the minimum efficiency requirements. With this constraint, five different PFC converters are used for comparison. Conventional PFC scheme used boost converter in CCM is excluded due to expensive PFC control IC. First and second converters are single stage PFC converters which are integration of boost converter in DCM and forward converter, and half-bridge converter in CCM respectively. Third, fourth and fifth converters are all two stage PFC converters. Third converter is consisted of the boost converter in critical conduction mode with frequency control and forward converter in CCM. Fourth converter has the boost converter in DCM with an additional PWM controller. Fifth proposed converter has a proposed single controller using delay control. The results of trade-off study are shown in Table I.

This trade-off study shows that a single stage, single-switch scheme is not a good candidate for the 200 W power supply in a Personal Computer in terms of efficiency and cost [6]. In order to overcome the above mentioned problems in single switch circuits, a two switch scheme with a single PWM controller is proposed. It resembles conventional two stage schemes. However a single PWM controller with an adaptive delay scheme drives the switches for both the PFC part and the dc–dc converter part differently to keep the capacitor voltage within the optimal range and to reduce the input current distortion. In Section II, the proposed scheme is described and its operating principle is explained. The design procedure of the delay control scheme and the loss analysis is summarized in Section III. Section IV presents the design of the feedback loop for the proposed PFC converter taking into consideration of the second harmonics of the input voltage and the input current distortion. In Section V, selected experimental verifications are presented.

II. OPERATING PRINCIPLES

The circuit diagram of the proposed SC PFC converter employing the delay control is shown in Fig. 1. The converter has a PFC switch, Q1 synchronized with the switch, Q2 of the cascaded forward converter. The switch, Q2 is controlled to regulate the dc output voltage by PWM controller. The switch, Q1 is controlled to keep the capacitor voltage within a desired range, depending on the operating condition and to reduce input current harmonic distortion. As can be seen in Fig. 1 the inputs of the delay controller are the gate drive signal for Q2 (GS2),

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